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10/720,437	11/24/2003	Thomas Vogelsang	2002 P 12738 US	5122

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EXAMINER	
STOYNOV, STEFAN	
ART UNIT	PAPER NUMBER
2116	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/720,437	VOGELSANG, THOMAS	
	Examiner	Art Unit	
	Stefan Stoynov	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 22-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *22-26* is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

The rejections for claims 1-15 are respectfully maintained and reproduced infra for applicant's convenience.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katsuhisa, US Patent No. 6,278,652 in view of Benno et al., US Patent Appl. Pub. No. 2003/0226054. Katsuhisa and Benno show all claim limitations in Figures 1-4 and 1-16, accordingly.

Regarding claim 1, Katsuhisa discloses a clock filter for an electronic device, the clock filter comprising:

a clock receiver 11 electrically coupled to an external clock CLK (column 1, lines 43-45, column 6, lines 6-10); and

an enabling circuit 4 electrically coupled to an external clock (column 6, lines 1-19);

wherein the clock receiver generates an internal clock signal (column 3, lines 9-15).

Katsuhisa fails to disclose the enabling circuit disables the clock receiver for a first time period after detecting a transition on the internal clock.

Benno teaches a clock filter similar to the current application (paragraph 0024, lines 1-3). Benno further teaches HOLDING CIRCUIT 203 and an exclusive-OR 205 (i.e. an enabling circuit), receiving both the internal clock and the control signal S21 for disabling the internal clock S12 transitioning for a predetermined period of time (paragraph 0073 – paragraph 0079, FIG. 3). Thus, both the internal clock transitions S12 and the signal indicative of noise S13 are detected and the receiver is stopped, accordingly. In Benno, the designer can change the period during which the internal clock signal is disabled with flexibility, thus preventing operation under unstable conditions due to external noise (paragraphs 0022 and 0035).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the enable circuit and the process of disabling the internal clock, as suggested by Benno with the clock filter disclosed by Katsuhisa in order to implement the enabling circuit disables the clock receiver for a first time period after detecting a transition on the internal clock. One of ordinary skill in the art would be motivated to do so in order to prevent operation under unstable conditions due to external clock noise.

Regarding claim 2, Benno further teaches the clock filter, wherein the enabling circuit includes a pulse generator 203 (HOLDING CIRCUIT 203 outputs pulse – see FIG. 3, S21).

Regarding claim 3, Benno further teaches the clock filter as per claim 2, wherein the pulse generator is electrically coupled to the clock receiver (output S83 of HOLDING CIRCUIT 203 coupled through gate 303, FIG. 12), and the pulse generator generates a pulse

signal S83 having a duration substantially equivalent to the first time period (S12 in FIG. 13 between T_{noise} and T_{n+2}, paragraphs 0142 and 0143).

Regarding claim 4, Benno further teaches the clock filter as per claim 3, wherein the clock receiver is disabled when the pulse signal is high (pulses S21, S32, and S83 in FIG(s) 3, 5, and 13, accordingly).

Regarding claim 5, Benno further teaches the clock filter, wherein the enabling circuit is electrically coupled to a clock filter enable signal (HOLDING CIRCUIT receiving signal S13, FIG(s) 2, 4, and 12).

Regarding claim 6, Benno further teaches the clock filter as per claim 5, wherein the enabling circuit disables the clock receiver when the clock filter enable signal is enabled (paragraph 0064).

Regarding claim 7, Katsuhisa discloses a clock filter for an electronic device, the clock filter comprising:

a clock receiver 11 electrically coupled to an external clock signal CLK, the clock receiver generating an internal clock signal (column 1, lines 43-45, column 6, lines 6-10);

Katsuhisa fails to disclose a pulse generator electrically coupled to the clock receiver, the pulse generator generating a pulse for a first period upon detecting a transition in the internal clock signal; and an enabling circuit coupled to the pulse generator and the clock receiver, the enabling circuit being electrically coupled to a clock filter enable signal and disabling the clock receiver for a duration of the first time period when the clock filter enable signal is enabled.

Benno teaches a clock filter similar to the current application (paragraph 0024, lines 1-3). Benno further teaches pulse generator (HOLDING CIRCUIT) electrically coupled to the clock receiver (via gates 205 or 303), the pulse generator generating a pulse (S21, S32, or S83) for a first period after detecting a transition in the internal clock signal (period S12 in FIG(s) 3 and 5 between T_{noise} and T_{n+1} and between T_{noise} and T_{n+2} in FIG. 13); and an enabling circuit coupled (gates 205 or 303) to the pulse generator and the clock receiver (FIG(s) 2, 4, and 12), the enabling circuit being electrically coupled to a clock filter enable signal (S13 electrically coupled to gates 205 or 303 through the HOLDING CIRCUIT 203) and disabling the clock receiver when the clock filter enable signal is enabled during the first time period (paragraph 0064). In Benno, the designer can change the period during which the internal clock signal is disabled with flexibility, thus preventing operation under unstable conditions due to external noise (paragraphs 0022 and 0035).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the above-described circuit and process of disabling the receiver, as suggested by Benno with the clock filter disclosed by Katsuhisa in order to implement a pulse generator electrically coupled to the clock receiver, the pulse generator generating a pulse for a first period upon detecting a transition in the internal clock signal; and an enabling circuit coupled to the pulse generator and the clock receiver, the enabling circuit being electrically coupled to a clock filter enable signal and disabling the clock receiver for a duration of the first time period when the clock filter enable signal is enabled. One of ordinary skill in the art would be motivated to do so in order to prevent operation under unstable conditions due to external clock noise.

Regarding claim 8, Benno further teaches the clock filter, wherein the enabling circuit is electrically coupled to a clock enable signal S13, the enabling circuit disabling the clock receiver when the clock enable signal is reset (S13 is couple to the reset input R of latches 301, 302, and 801 in FIG(s) 4 and 12, paragraph 0091).

Regarding claim 9, Benno further teaches the clock filter, wherein the enabling circuit includes:

a NAND gate electrically coupled to the pulse generator and the clock filter enable signal; and

an AND gate electrically coupled to the NAND gate such that the output of the NAND gate is a first input to the AND gate

[Benno teaches logical gates (205 and 303) interconnected with the pulse generator and the clock filter enable signal (FIG(s) 2, 4, and 12). Although the gates and connection taught by Benno are not identical to the gates and interconnections, as indicated above, the achieved functionality is the same as in the claimed invention. Thus, Benno teaches obvious variations for implementing the same functionality by utilizing different logic gates].

Regarding claim 10, Benno further teaches the clock filter as per claim 9, wherein the AND gate has a second input electrically coupled to a clock enable signal.

Regarding claim 11, Benno further teaches the clock filter as per claim 9, wherein an output of the AND gate is electrically coupled to the clock receiver.

Regarding claim 12, Benno further teaches the clock filter, wherein the enabling circuit includes:

a first NAND gate electrically coupled to the pulse generator and the clock filter enable signal;

a second NAND gate electrically coupled to an output of the first NAND gate; and

an inverter electrically coupled to an output of the second NAND gate, wherein the output of the inverter is electrically coupled to the clock receiver.

[Benno teaches logical gates (205 and 303) interconnected with the pulse generator and the clock filter enable signal (FIG(s) 2, 4, and 12). Although the gates and connection taught by Benno are not identical to the gates and interconnections, as indicated above, the achieved functionality is the same as in the claimed invention. Thus, Benno teaches obvious variations for implementing the same functionality by utilizing different logic gates].

Regarding claim 13, Benno further teaches the clock filter as per claim 12, wherein the second NAND gate has a second input electrically coupled to a clock enable signal.

Regarding claim 14, Katsuhisa and Benno further teach the clock filter as per claim 12, wherein the first NAND gate has a second input electrically coupled to a test mode enable signal (Katsuhisa, TEST MODE SIGNAL, FIG(s) 1 and 4).

Regarding claim 15, Benno further teaches the clock filter, wherein the first time period is about 5% to about 10% of a transition period of the external clock signal (paragraph 0035).

Allowable Subject Matter

Claims 22-26 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 22, the prior art of record fails to disclose or suggest all the subject matter of claim 22, including "the pulse generator generating a second pulse signal for a

second duration upon detecting a transition in the internal clock signal, the second duration being less than the first duration; and the enabling circuit disabling the clock receiver via the clock receiver enable signal during the second duration if the clock enable signal is enabled".

Response to Arguments

Applicant's arguments filed 12/20/2006 have been fully considered but they are not persuasive.

Regarding claim 1, the applicant argued that neither the Katsuhisa nor the Benno reference teach the enabling circuit disables the clock receiver for a first period of time after detecting a transition on the internal clock signal.

Regarding claim 7, the applicant argued that the Benno reference does not teach the pulse generator generating a pulse signal for a first time period upon detecting a transition in the internal clock signal.

The examiner respectfully disagrees.

With regards to claim 1, in FIG. 3, Benno teaches transitioning the internal clock signal S12 from "low" to "high" at T_3. Afterwards, due to noise the clock control circuit prevents the internal clock signal S12 from transitioning back to "low" at T_n (as expected under normal operation without noise – paragraph 0076, lines 1-4). Therefore, the clock control circuit has detected the previous transitioning (at T_3) of the internal clock signal and any further clock transitions are stopped at T_n by the enabling circuit (203 and 205) (paragraphs 0076-0077). As shown in FIG. 3, the internal clock signal is held at the same level ("high") in the period between T_{noise} and T_{n+1} (i.e. for a first period of time – paragraphs 0077 and 0078). During the

same time period the lack of internal clock signal further stops the operation of the internal circuit 103 (i.e. the clock receiver is disabled – paragraphs 0080-0082). In order to maintain the same level after the clock transition, the clock control circuit must necessarily detect the earlier transition of the internal clock signal and further to maintain the latest detected clock level for a first period of time after detecting a noise condition. Thus, Benno teaches the enabling circuit disables the clock receiver for a first period of time after detecting a transition on the internal clock signal and meets the claim language.

The same explanation applies with regards to claim 7, wherein the pulse generator (FIG. 2, HOLDING CIRCUIT 203) generates a pulse signal for a first period of time (FIG. 3, pulse S21 after detection of noise) upon (defined as "THEREAFTER", Merriam-Webster's Collegiate Dictionary, Tenth Edition 1999, page 1298, definition of word upon) detecting a transition in the internal clock signal, as indicated above.

Therefore, the rejection of claims 1 and 7 is maintained.

Dependent claims 2-6 and 8-15 stand rejected, as indicated in this Office action.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory

period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stefan Stoynov whose telephone number is (571) 272-4236. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

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3/8/07